

Fig. 1
(PRIOR ART)

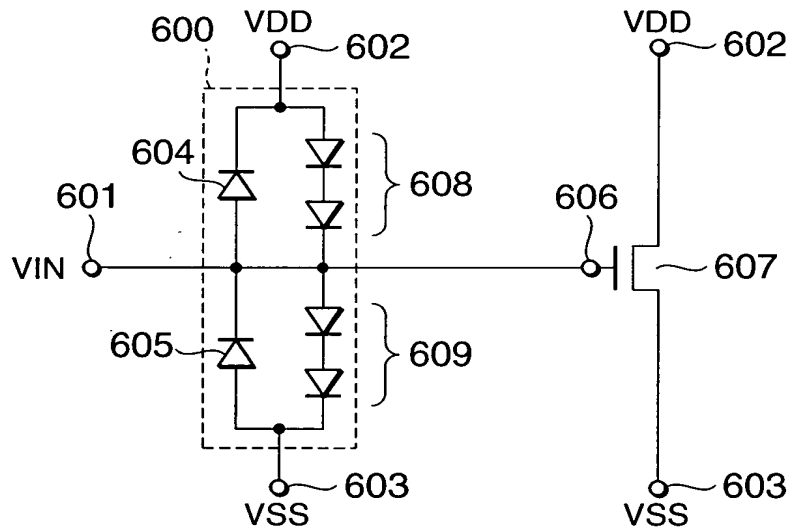


Fig. 2A
(PRIOR ART)

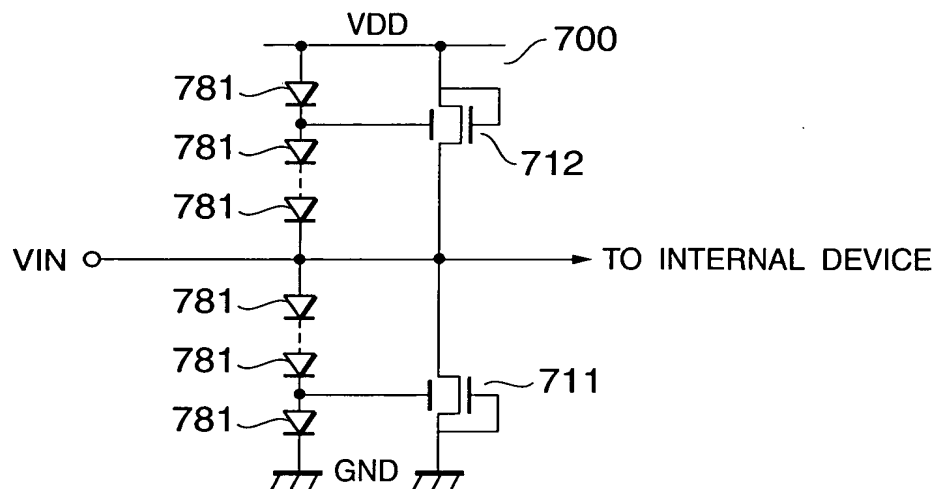
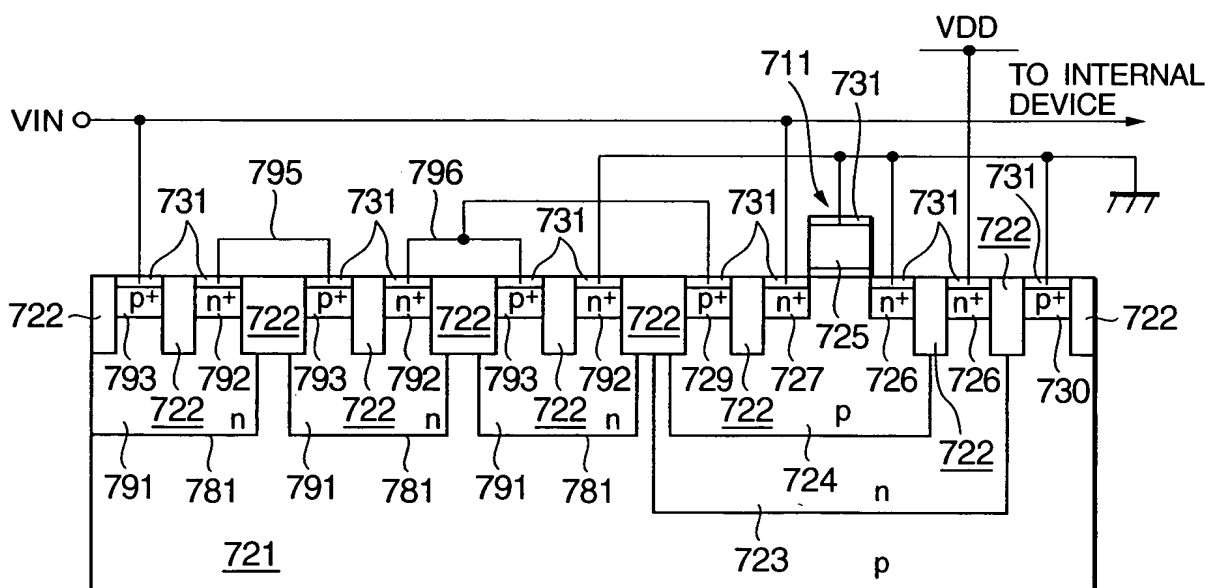


Fig. 2B
(PRIOR ART)



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Fig. 3A
 (PRIOR ART)

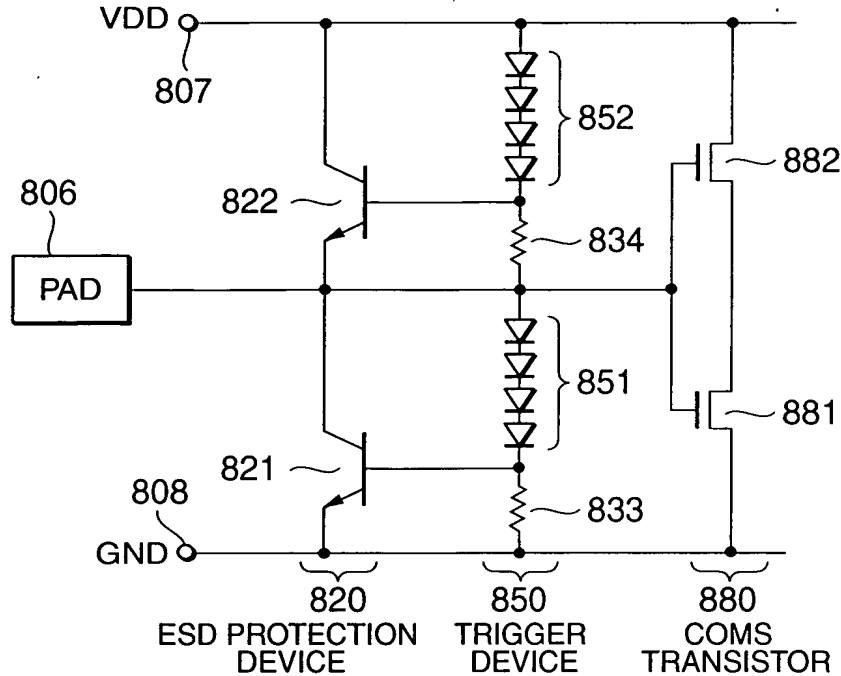


Fig. 3B
 (PRIOR ART)

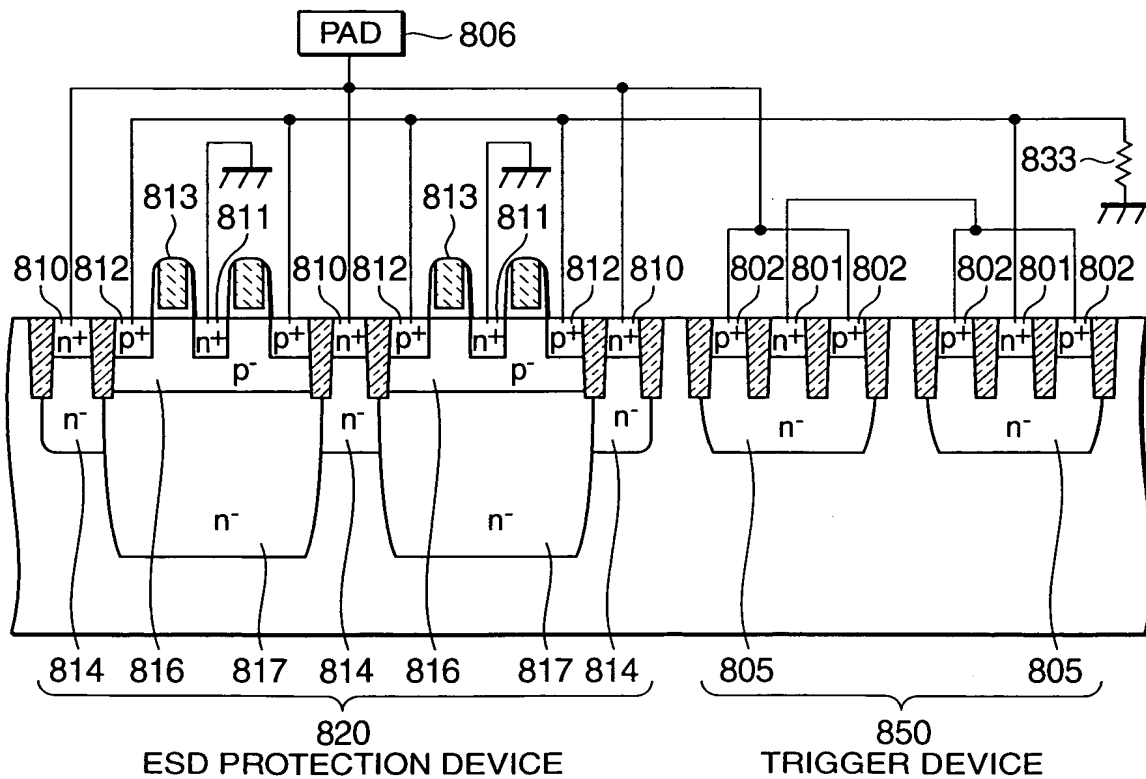


Fig. 4A
 (PRIOR ART)

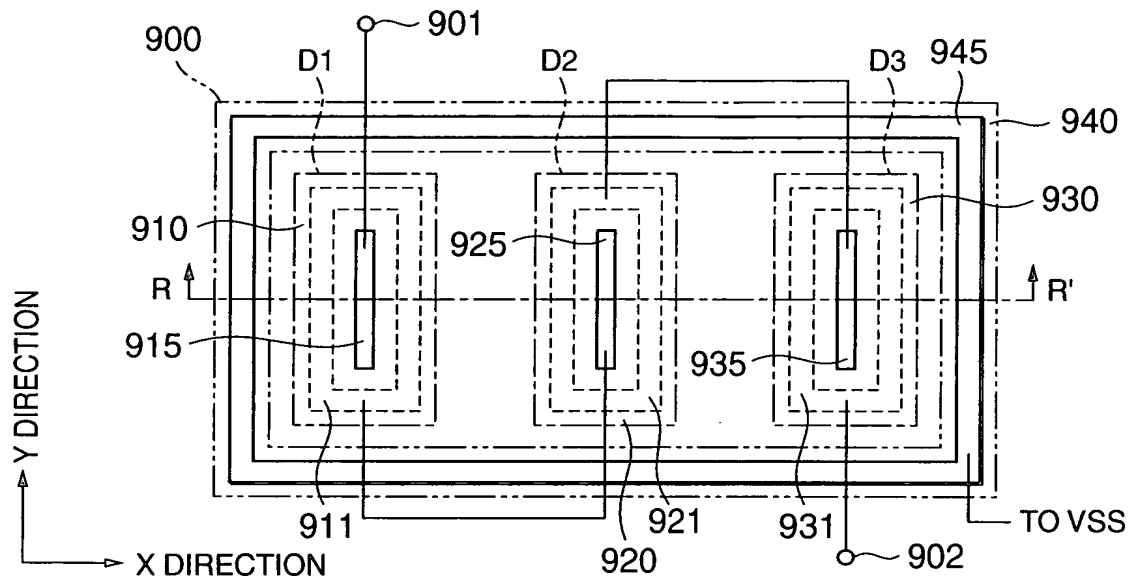


Fig. 4B
 (PRIOR ART)

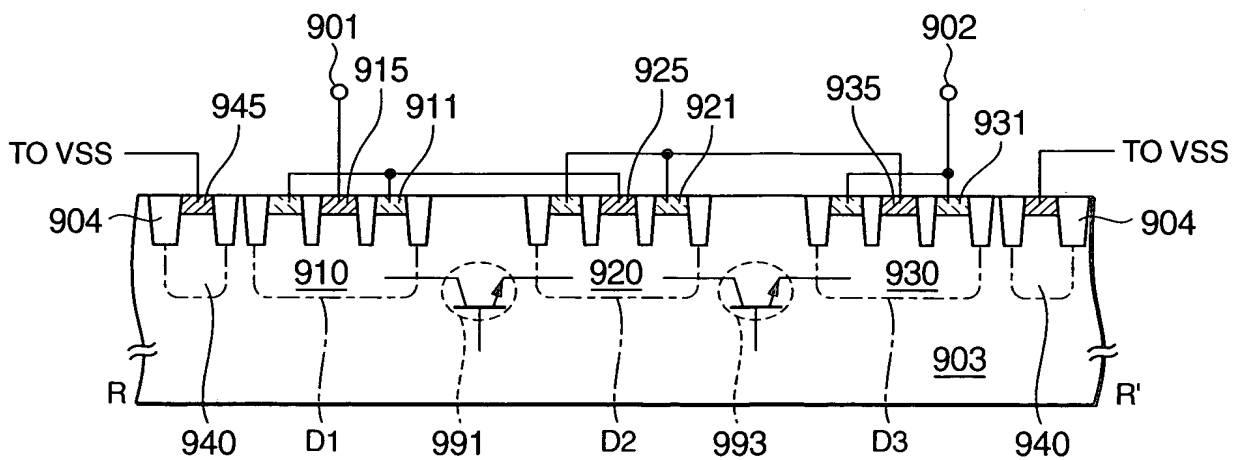
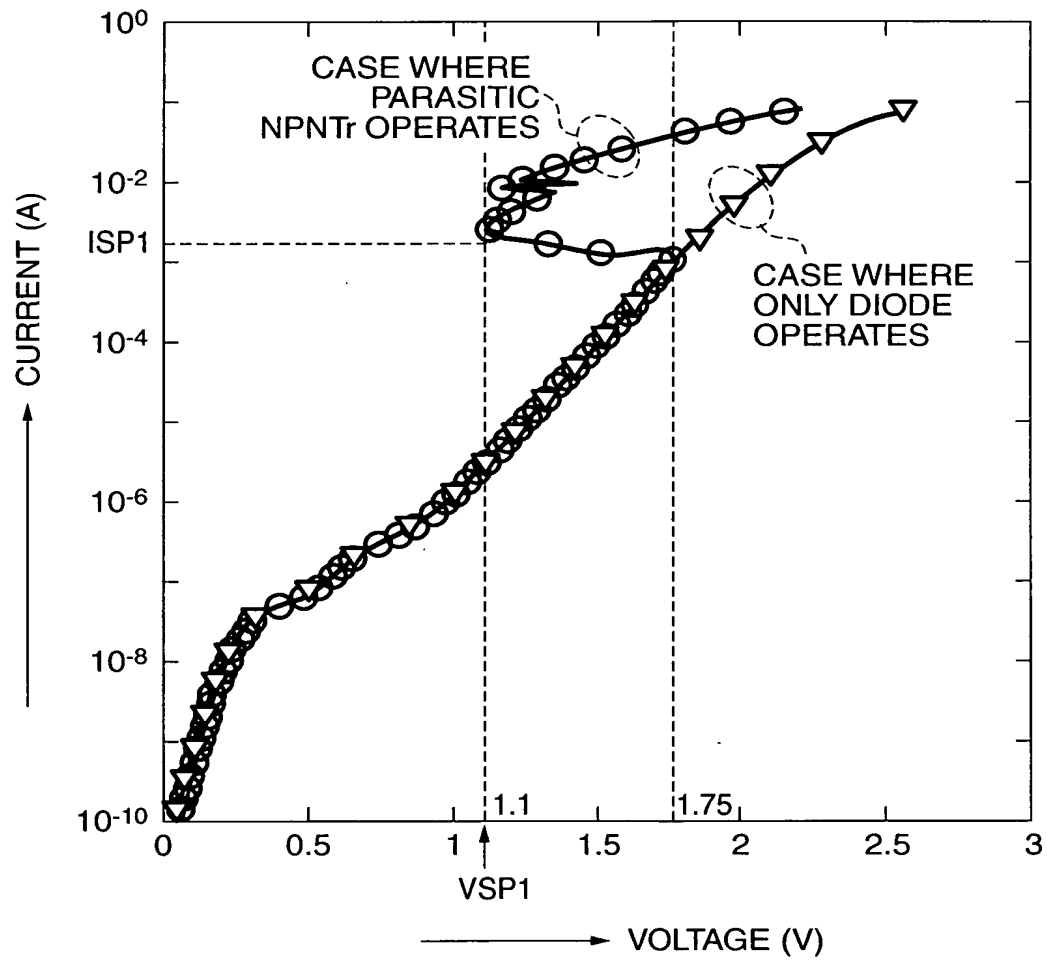


Fig. 5



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Fig. 6A

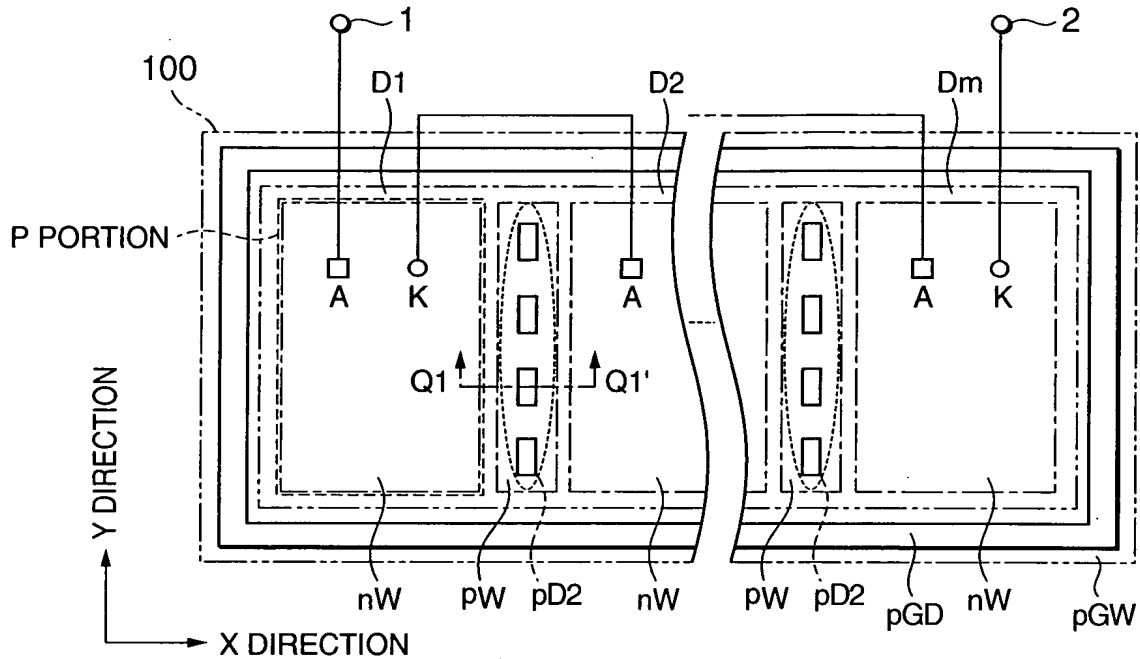


Fig. 6B

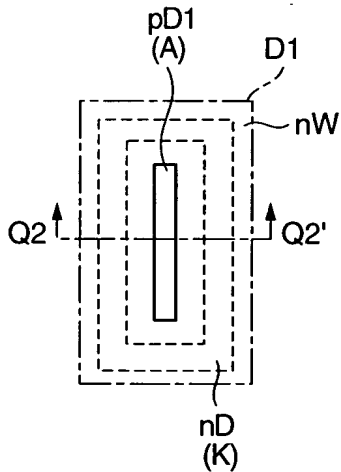


Fig. 6C

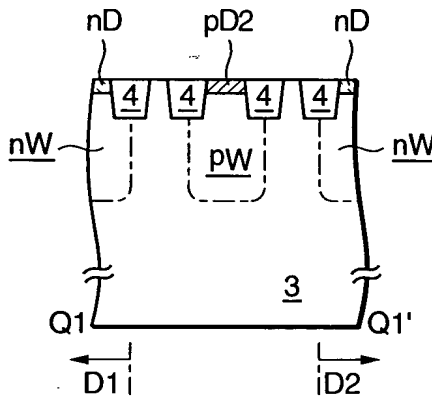


Fig. 6D

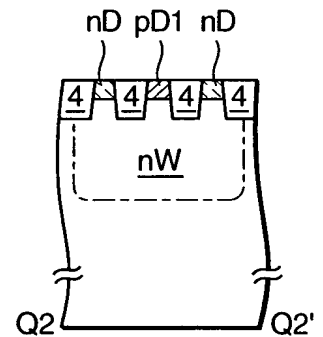
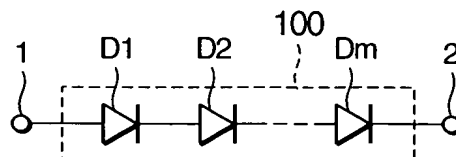


Fig. 6E



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Fig. 7A

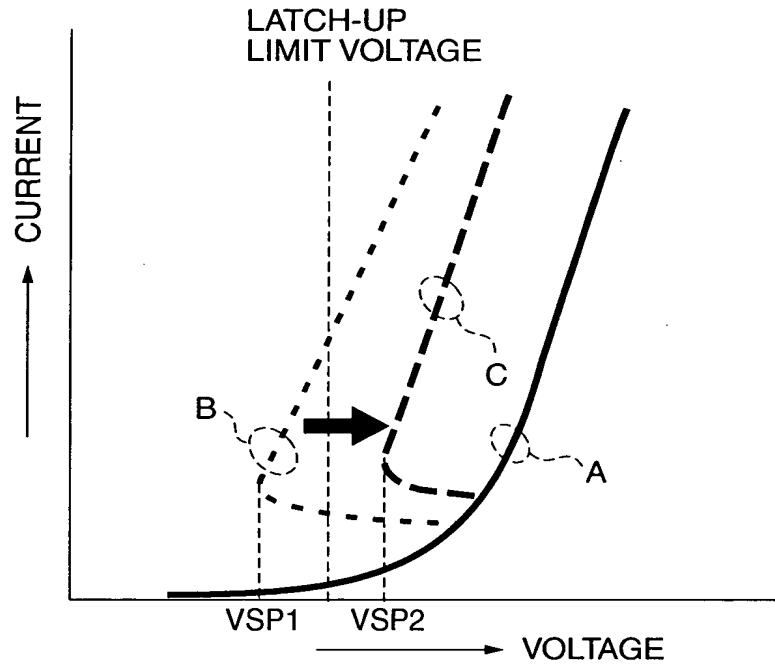
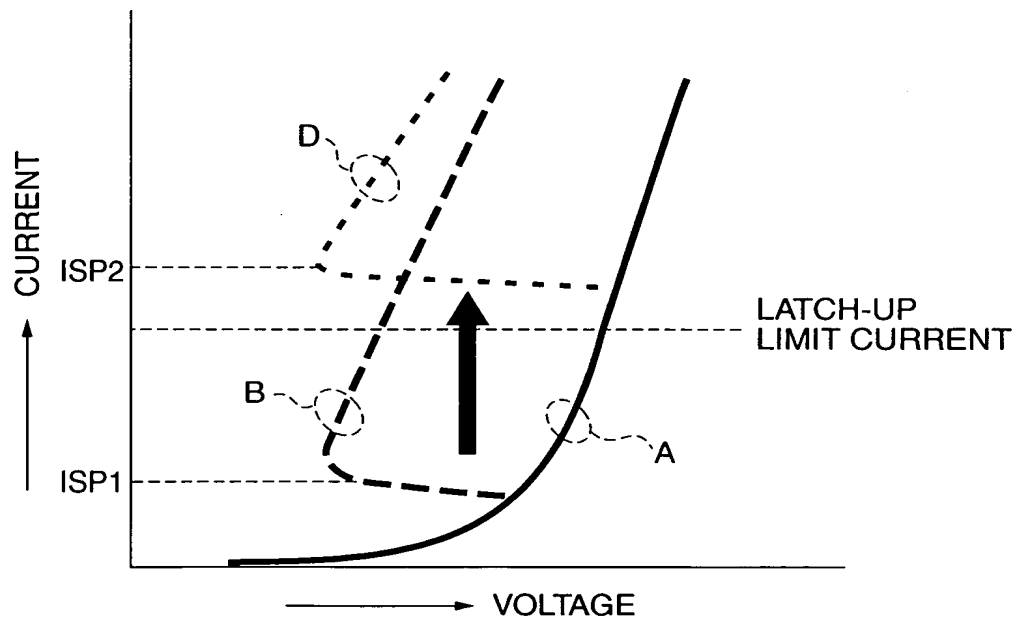


Fig. 7B



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Fig. 8A

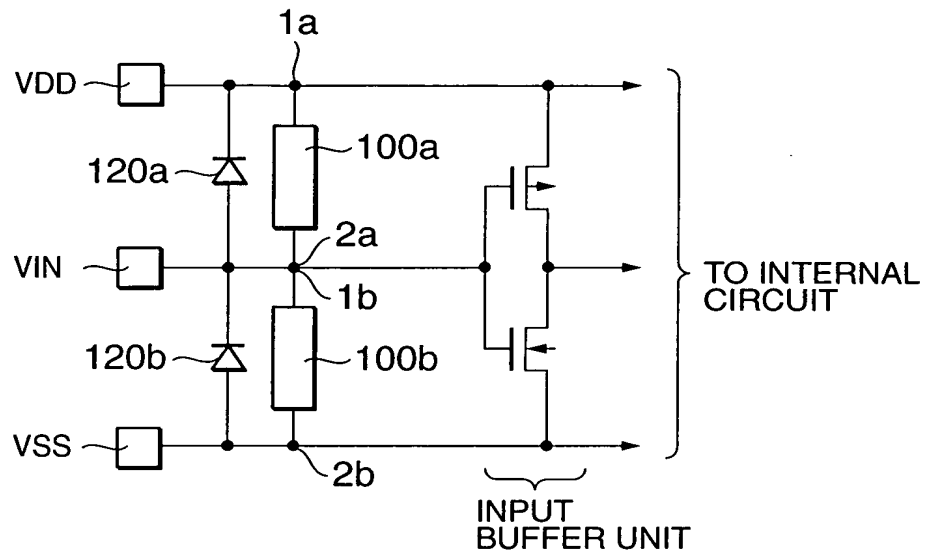


Fig. 8B

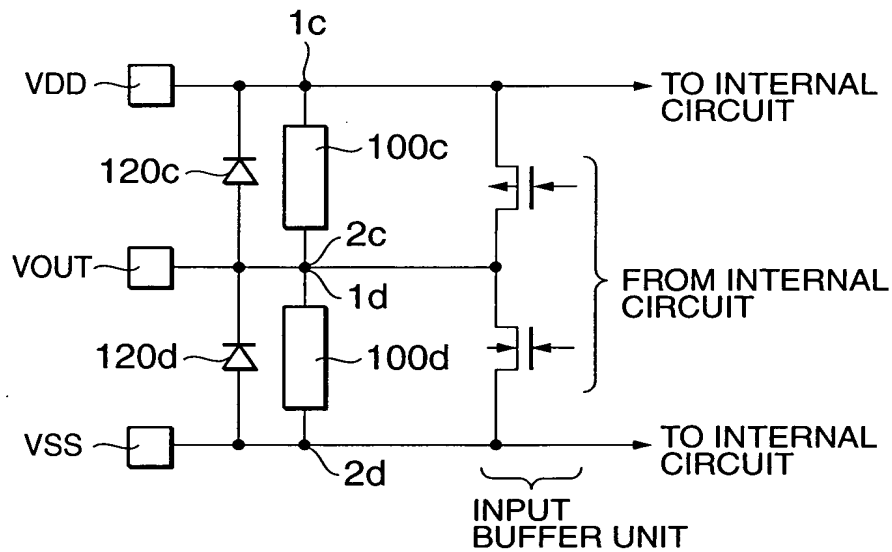


Fig. 8C

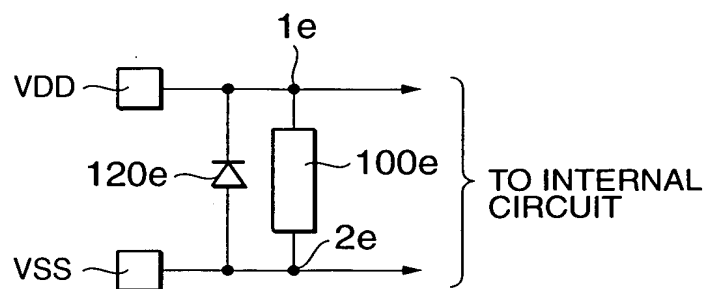


Fig. 9A

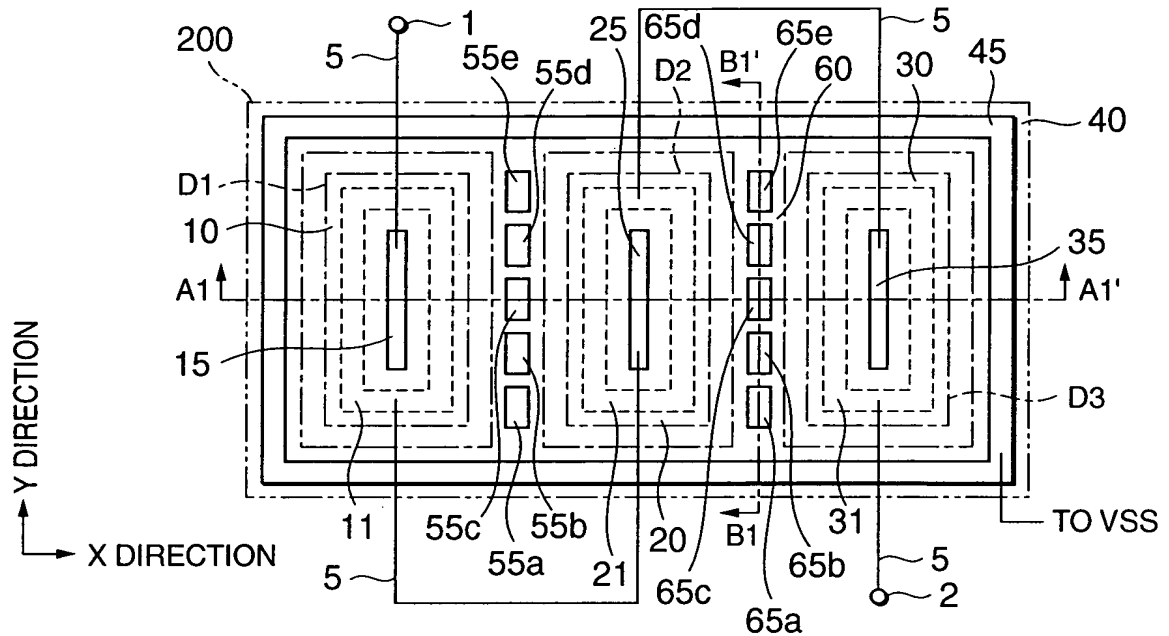


Fig. 9B

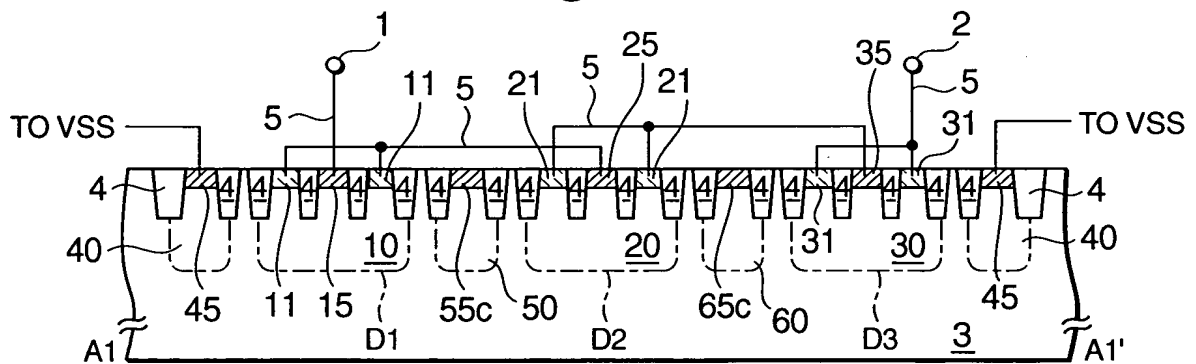
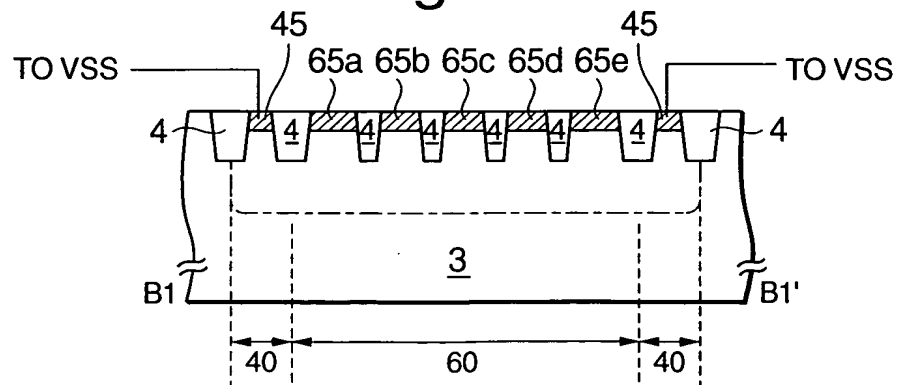


Fig. 9C



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Fig. 10A

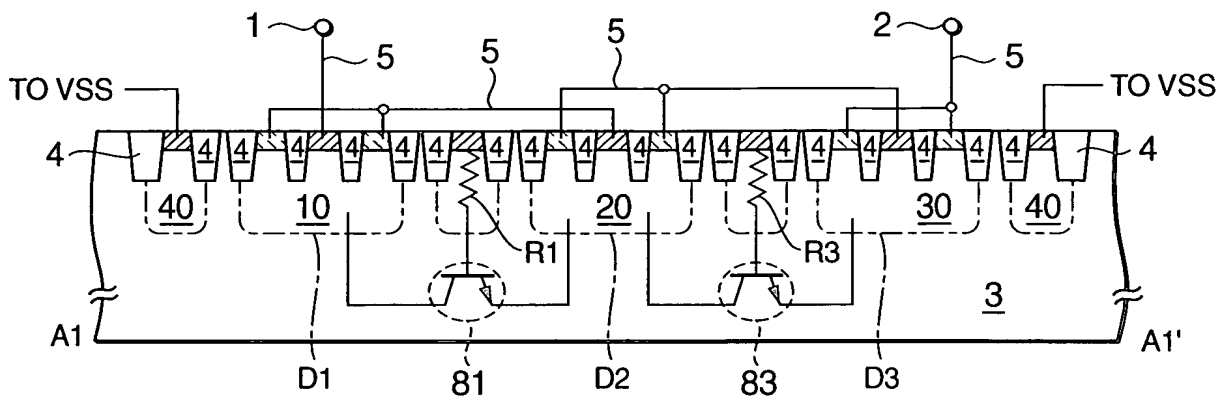


Fig. 10B

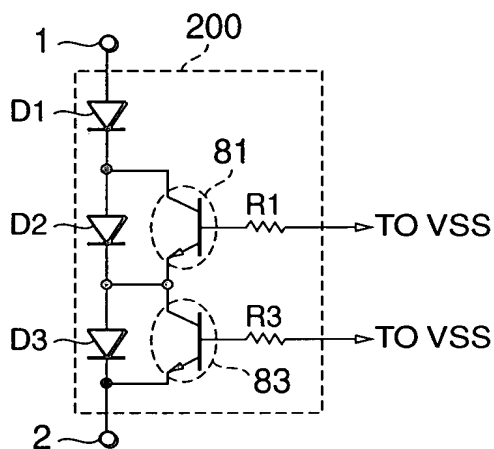


Fig. 10C

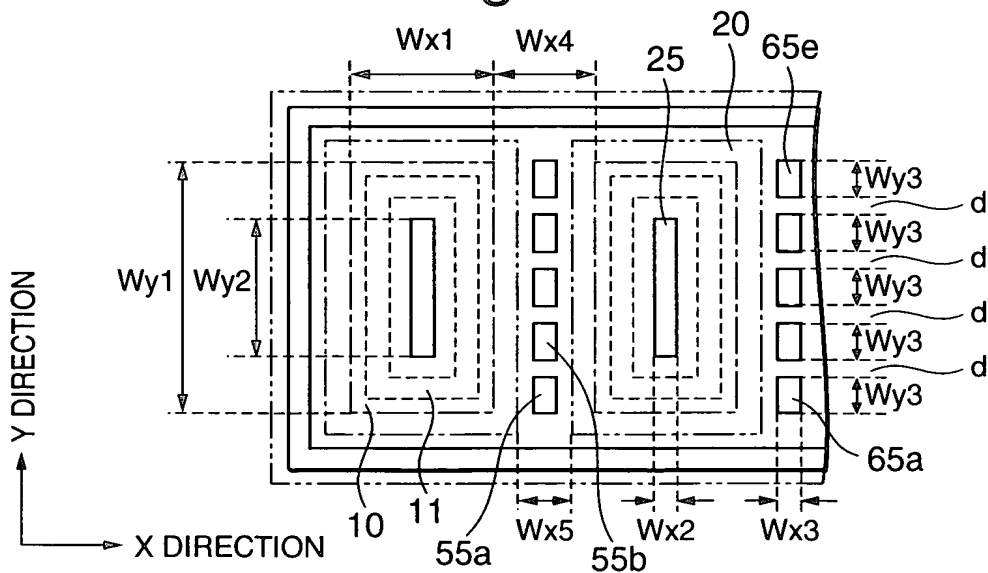


Fig. 11A

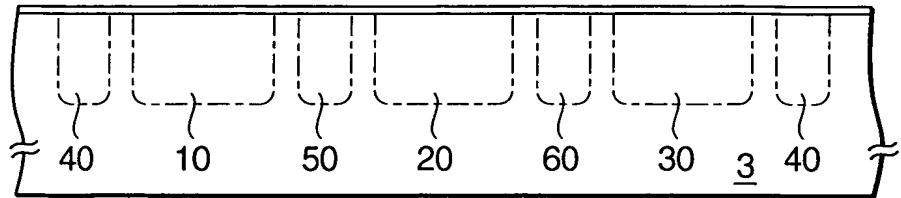


Fig. 11B

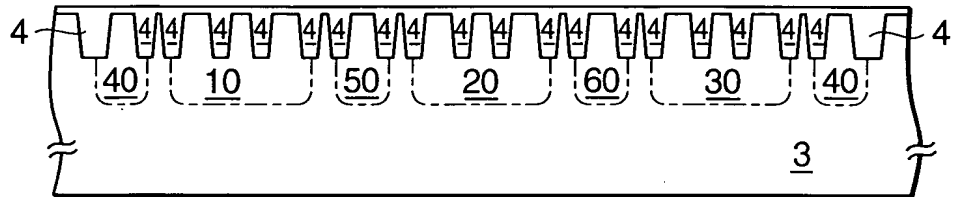


Fig. 11C

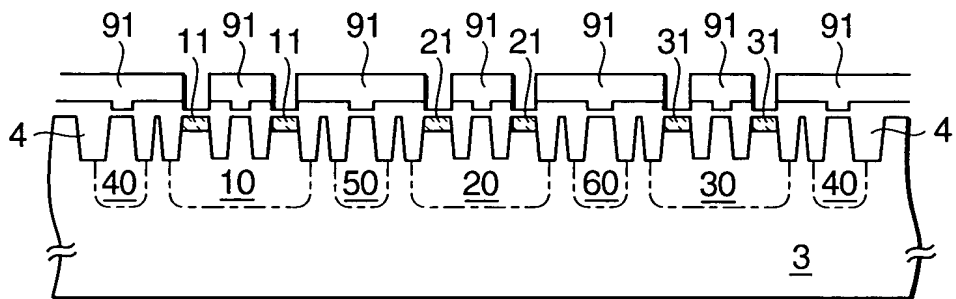


Fig. 11D

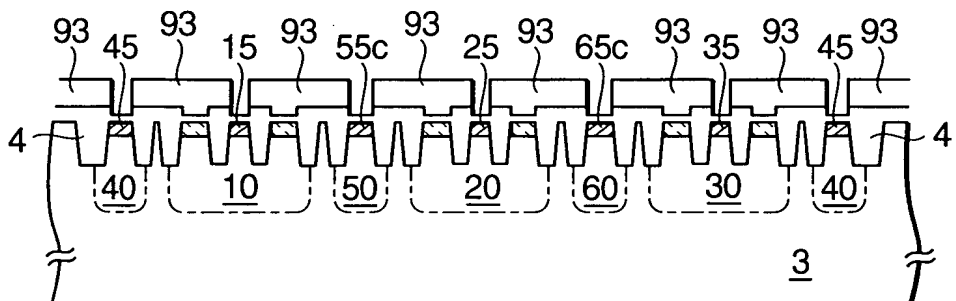
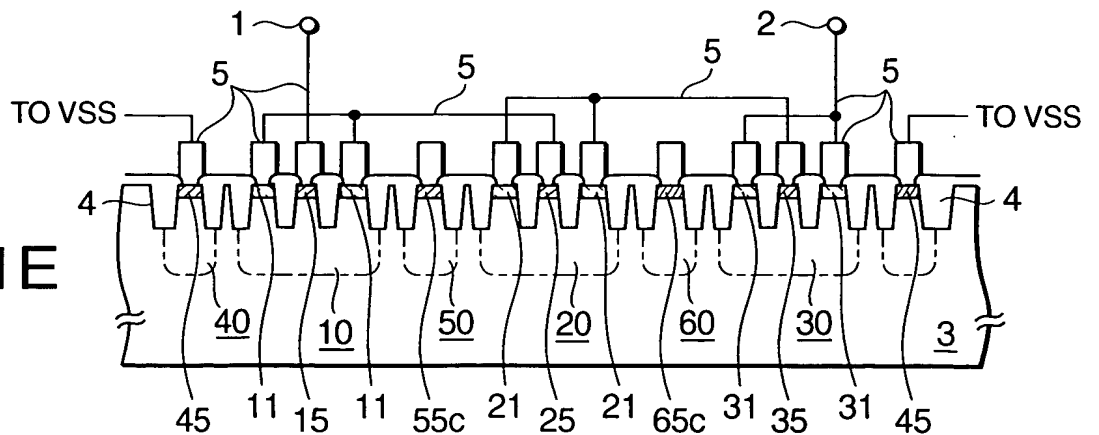
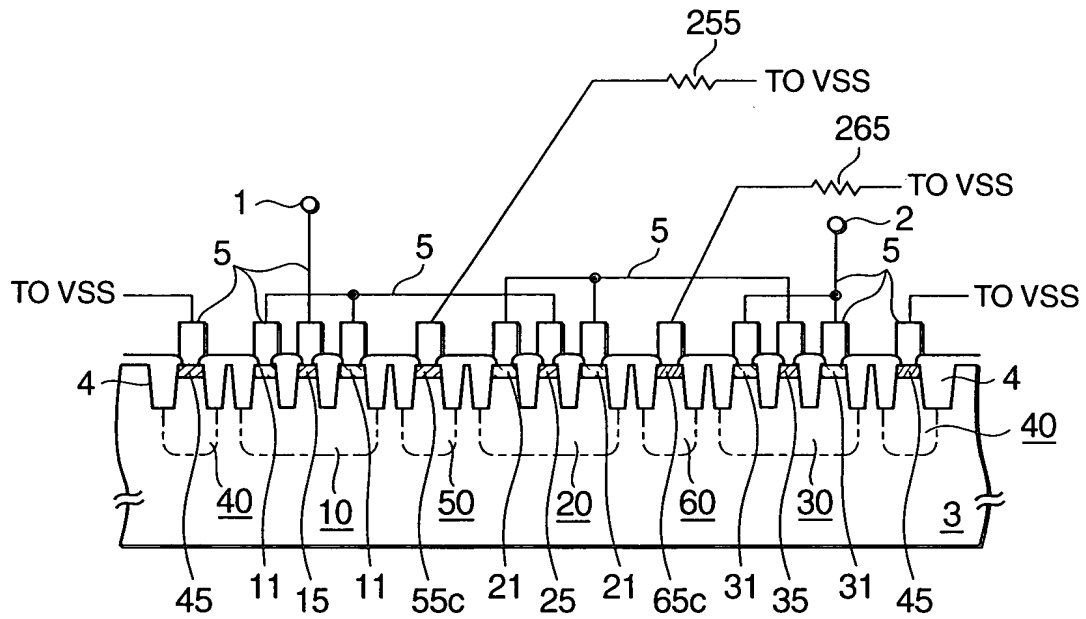


Fig. 11E



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Fig. 11G



[illegible]

Fig. 13A

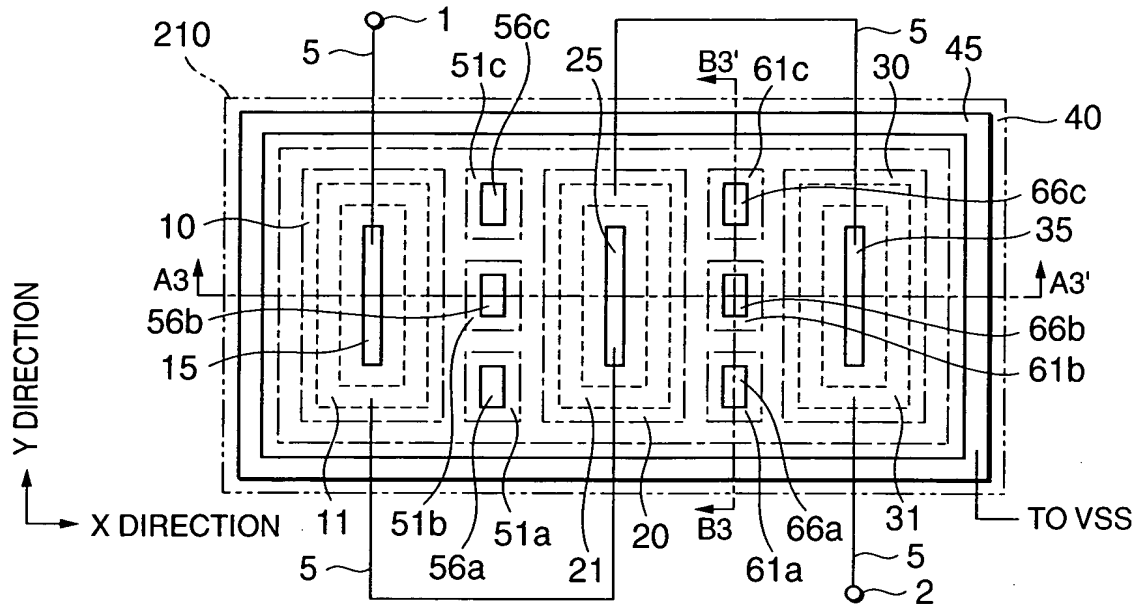


Fig. 13B

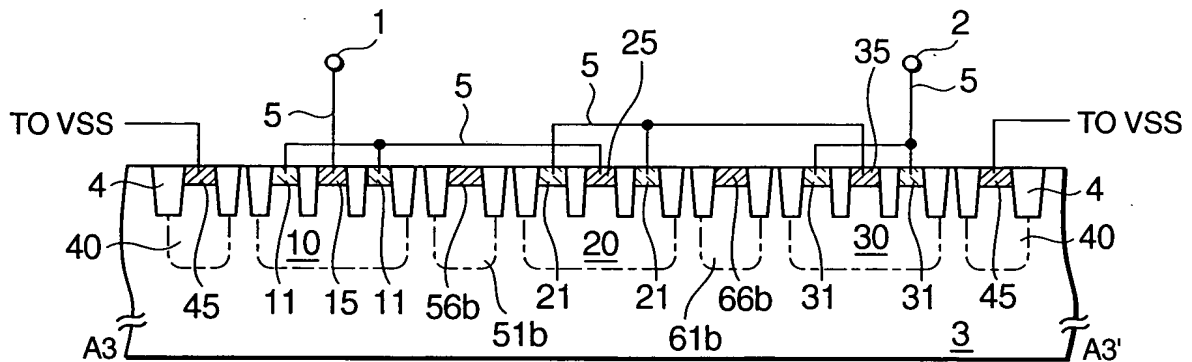


Fig. 13C

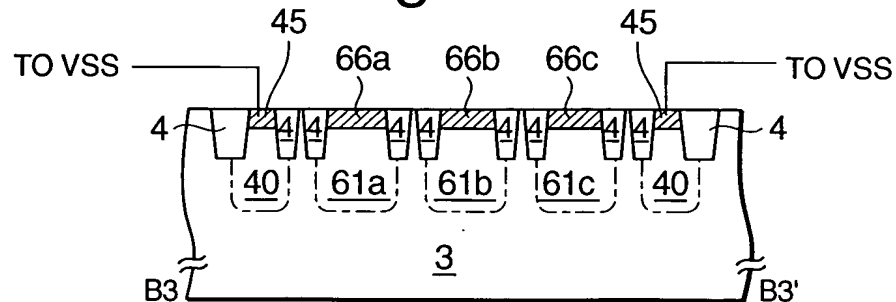


Fig. 14A

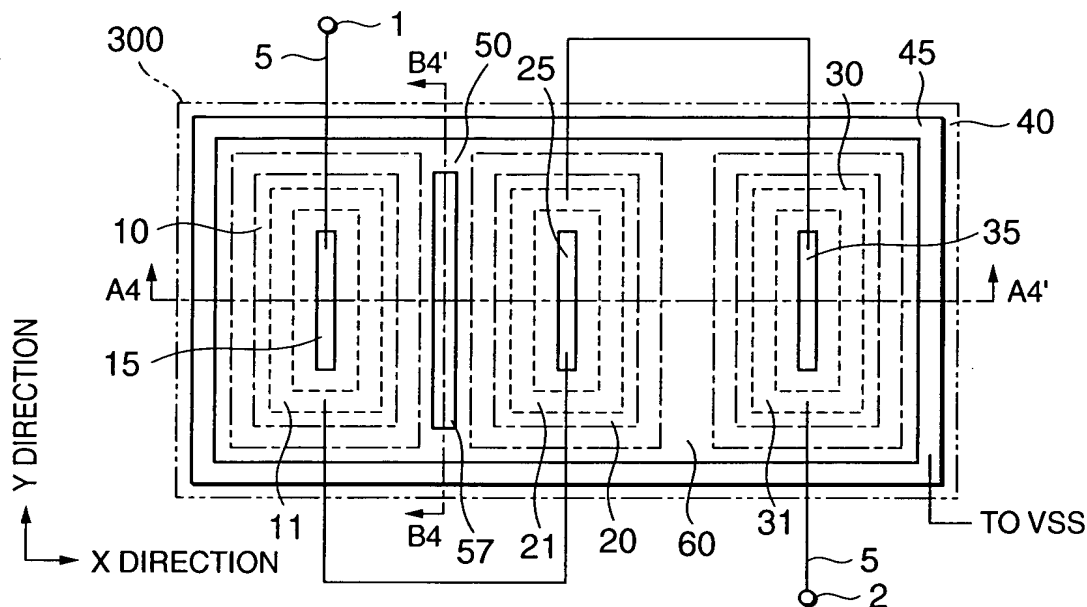


Fig. 14B

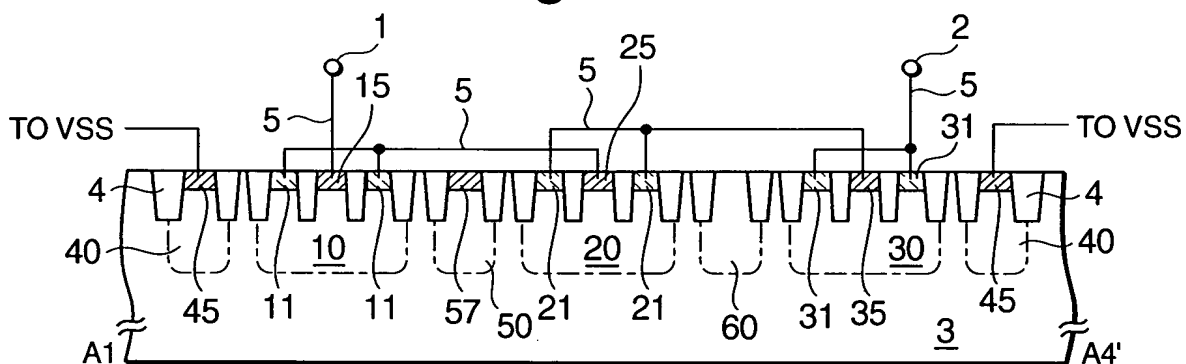
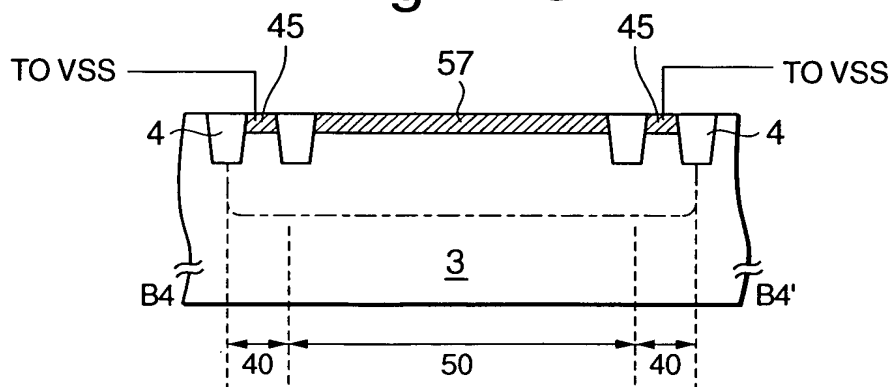


Fig. 14C



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Fig. 15A

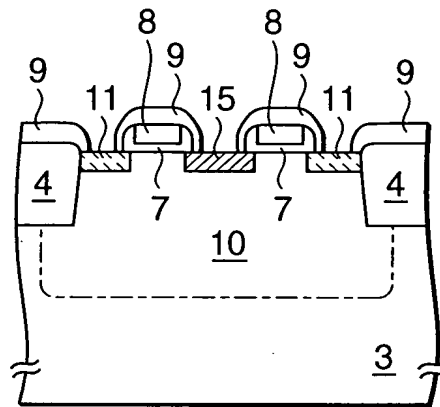


Fig. 15B

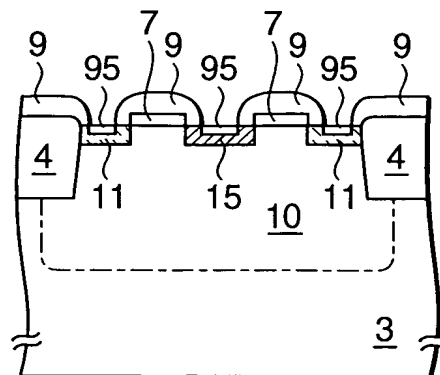


Fig. 3 is a cross-sectional view of a semiconductor device. It shows a series of gates (91) and contacts (4) on a substrate. The gates are separated by spacers (11). The contacts are connected to the gates. The device is shown in a perspective view, with a dashed line indicating a cross-section. The labels 91, 11, 8, 21, 31, 4, 40, 10, 50, 20, 60, 30, and 7 are used to identify various components.

A cross-sectional view of a semiconductor device. The device features a series of gates (93) on top of a substrate. The gates are separated by regions (45). The gates are connected to a common line (4). The regions (45) are connected to a common line (3). The gates are labeled with numbers 93, 45, 93, 15, 93, 55c, 93, 25, 93, 65c, 93, 35, 93, 45, 93. The regions are labeled with numbers 40, 10, 50, 20, 60, 30, 40. The gates are connected to a common line (4) and the regions are connected to a common line (3).

[illegible]

Fig. 17A

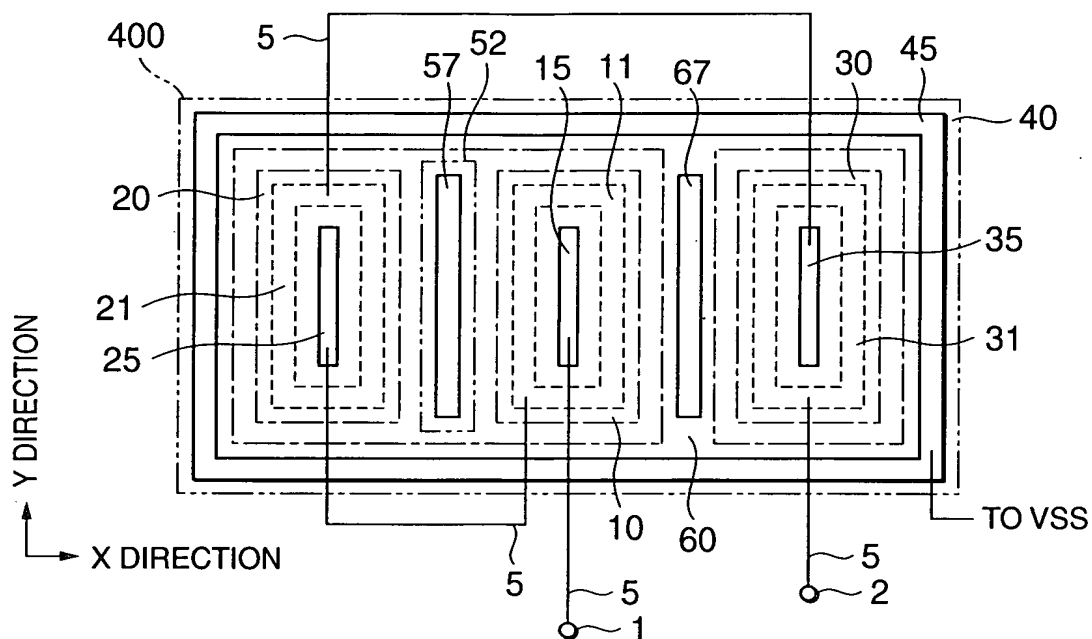


Fig. 17B

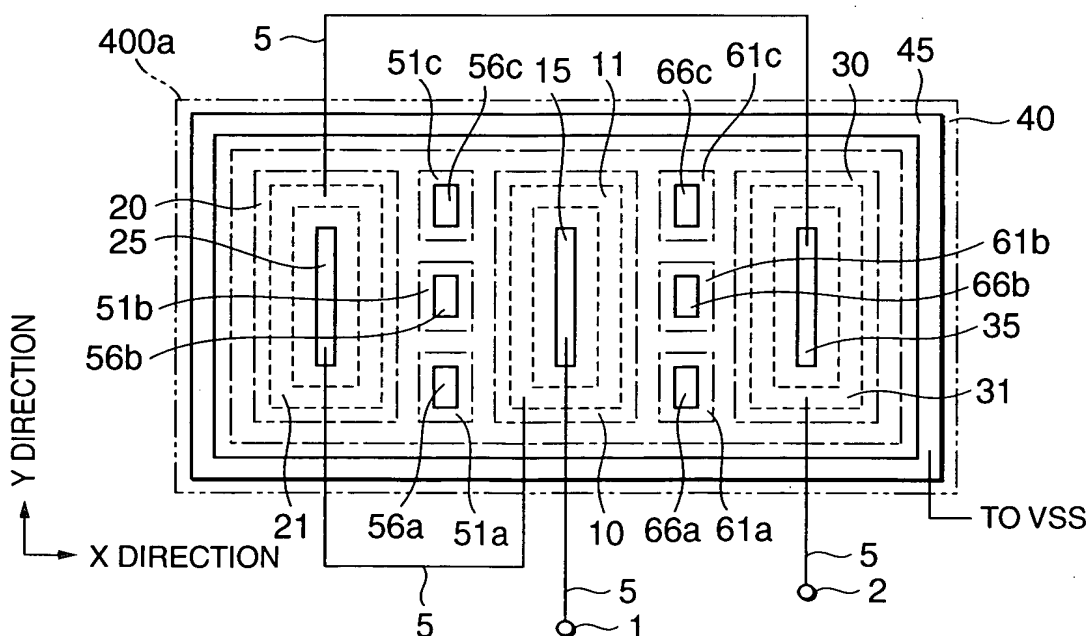


Fig. 18A

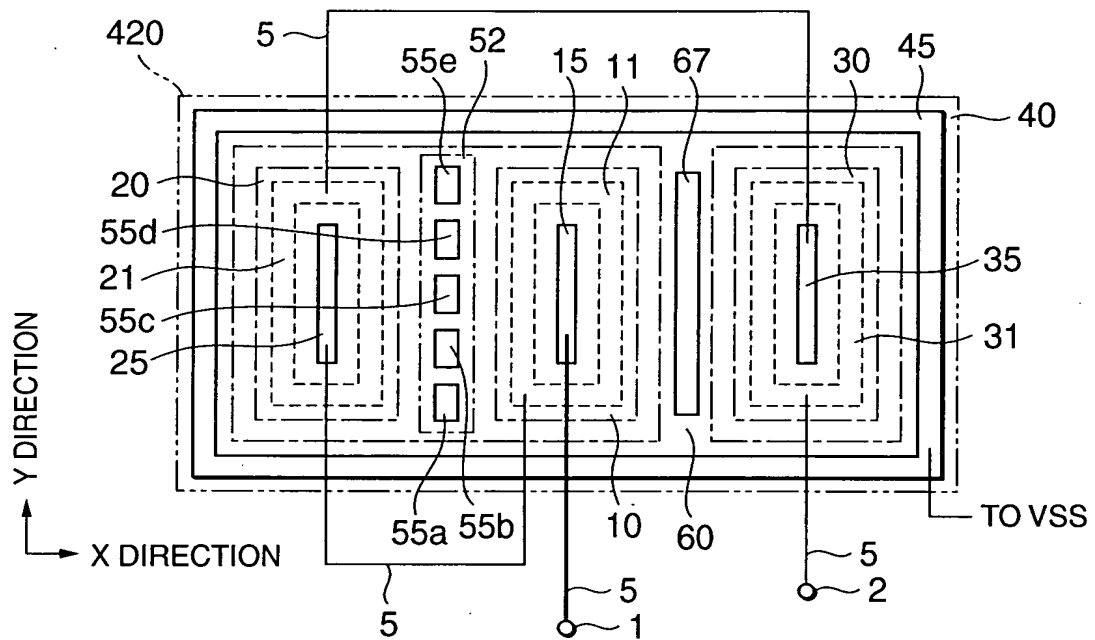


Fig. 18B

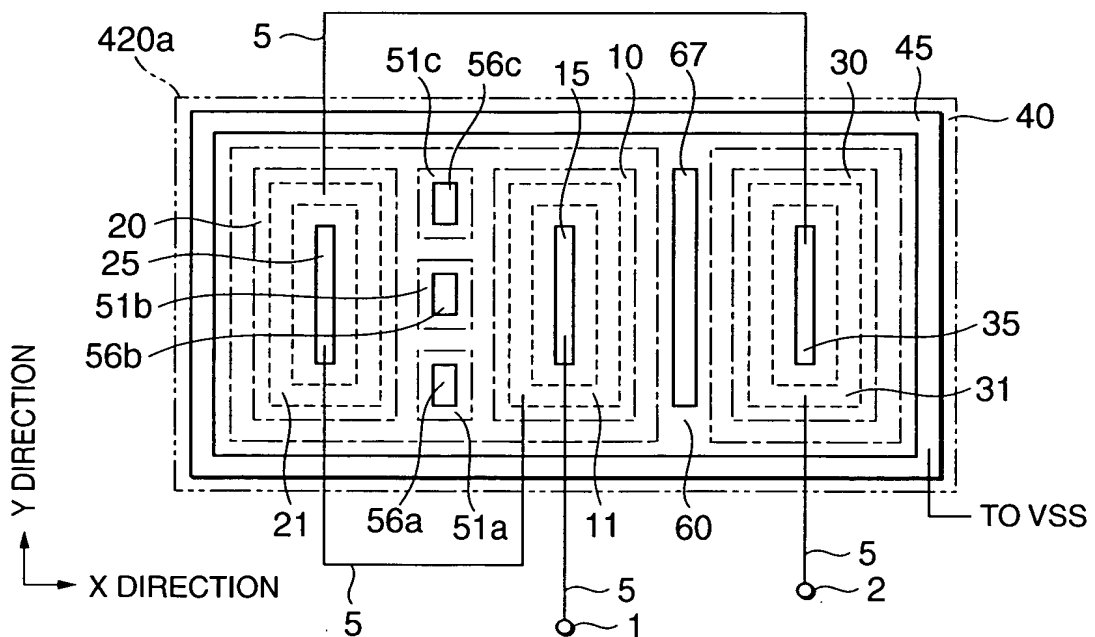
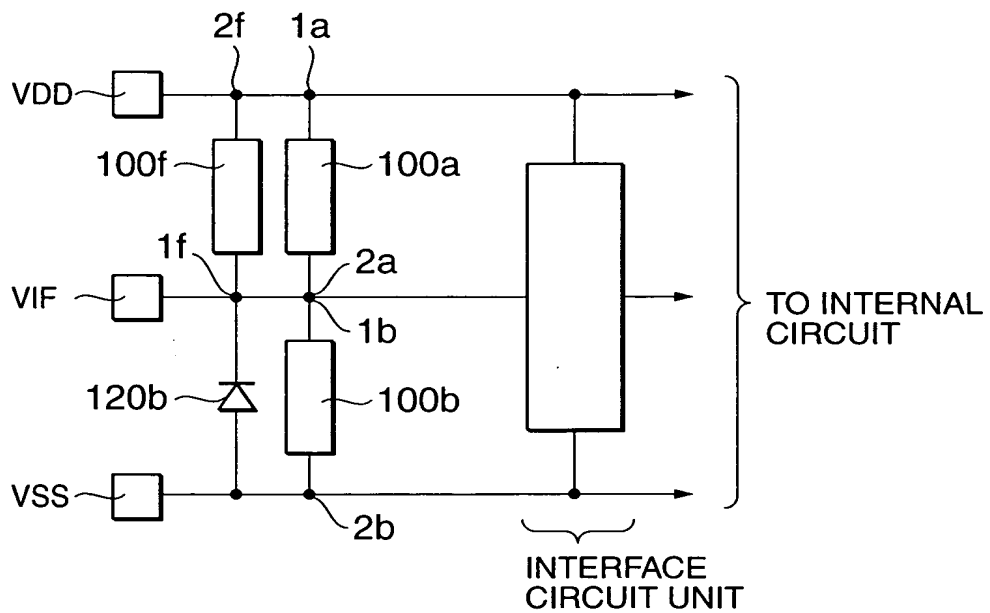


Fig. 19



INTERFACE CIRCUIT UNIT : INPUT BUFFER CIRCUIT,
OUTPUT BUFFER CIRCUIT AND THE LIKE